# Sweep Deflection Circuit Development Using Computer-Aided Circuit Design for the OMEGA Multichannel Streak Camera

A streak camera is an electro-optic instrument capable of resolving high-speed, low-repetition-rate, pulsed laser phenomena. The basis of the instrument is a streak tube. The image of the light to be analyzed is focused onto a photocathode at the input end of the streak tube. The photocathode emits electrons in response to the intensity of the light. The electrons, focused into a beam, are accelerated and deflected to a luminescent screen at the other end of the tube. This electron beam, impinging upon the screen, produces an intensified image of the light being analyzed. This image is then optically coupled to a CCD (charge-coupled device) imager, which digitizes the information for storage. To study the temporal variation of pulsed light a streak mode of operation is utilized whereby the electron beam is swept across the phosphor at a predetermined rate to provide the dimension of time along the axis of the swept image. To sweep the electron beam a pair of electrostatic deflection plates are provided in the streak tube (see Fig. 73.8). The position of the beam is linearly related to the voltage potential on the deflection plates. A linear voltage ramp is applied to the deflection plates to produce a linear sweep with respect to time. The sweep deflection circuit described produces the voltage ramp needed for the temporal study of the beams within the OMEGA system.

The multichannel streak camera is being developed at LLE to measure multiple-beam power balance and timing following the 3$\omega$ frequency-conversion crystals on OMEGA. The camera design is built around a commercial streak tube.[1] The primary design goal is to be able to perform a temporal display of ten OMEGA beams simultaneously along with two fiducial timing beams. With six of these cameras all 60 OMEGA beams can be analyzed simultaneously. Other goals include remote automated operation, fiber-optic light interface to the photocathode, and a highly reliable modular design. The modular design is required to facilitate serviceability and minimize down time in the event of circuit failure. Circuit malfunctions can be quickly diagnosed to the module level and a functioning module can then be interchanged without significant recalibration of the instrument. The sweep module and streak camera frame are shown in Fig. 73.9.

Functionally the streak camera sweep module circuitry must synchronously output a bipolar, high-voltage ramp with a duration of 6 ns. The magnitude of the total end-to-end differential sweep voltage, as seen between the two deflection plates, is approximately 2000 V. This translates to a sweep of the electron beam across 40 mm of the streak tube display. Because errors in the linearity of the output ramp voltage translate directly to measurement errors in time resolution of the instrument, it is important to minimize deviations in the slope of the differential ramp voltage.

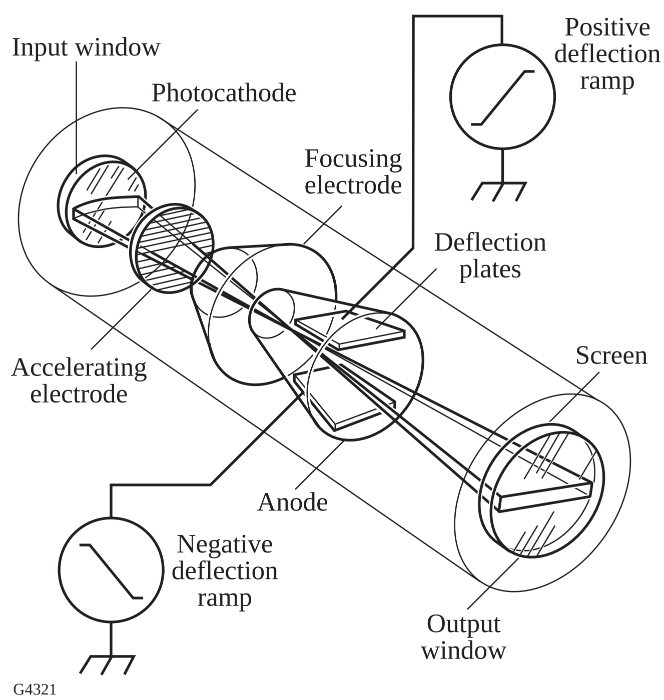


Figure 73.8
Streak tube schematic with deflection ramp sources.[1]

(a)

(b)

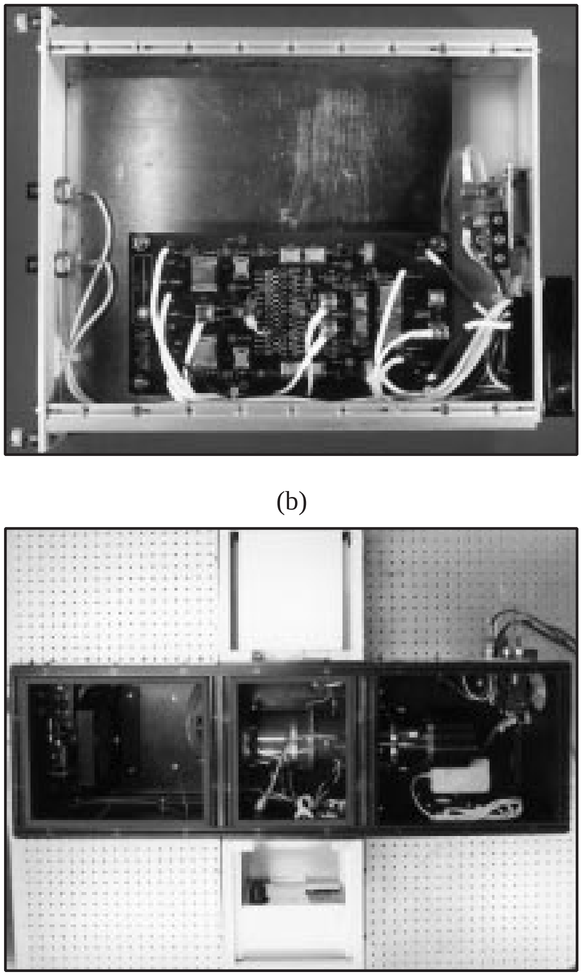

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Figure 73.9
OMEGA multichannel streak camera: (a) sweep module and (b) streak camera frame.

The 6-ns sweep ramp is a high-bandwidth signal that requires care in design to account for nonideal component behavior. The particular problems encountered center around the stray reactive components, also known as parasitics, that are inherent in all electronic components. These parasitics are not usually a problem in low-frequency designs (<1 MHz) but become a significant contribution to performance, or lack thereof, in higher-frequency designs. The development of the streak camera sweep circuit accounts for the parasitics of the components to determine and correct for their effects. A circuit design accounting for all parasitics can become nearly impossible to solve in closed form resulting from the complexity of the component parasitic models. To aid in the design, a circuit simulator computer program is used to model the circuitry with parasitics.

The modular design approach used here, while it does provide serviceability, requires additional mechanical interface complexity within the system interconnect structure. The interface complexity results from added connectors and increased wiring length to accommodate packaging. These extra wire lengths and added connectors introduce additional parasitic elements into the circuit interface that degrade high-bandwidth performance and must be accounted for in any modeling.

The goal of the sweep module design is achieved through the use of computer-aided analysis of the circuit design. The computer model includes parasitics that contribute to nonideal behavior. The initial design is conducted using this model. From the initial design a first-pass circuit "breadboard" is built and tested. An increasing complexity of parasitic elements is included until the model output compares to the actual breadboard circuit performance. With the model output matching the actual circuit, a rapid investigation of ways to optimize performance can then be accomplished. Also, anomalies in the circuit operation and performance measurement system can be analyzed. Although the main emphasis for use of the computer circuit model is to understand and correct the effects of the parasitics, it is also a valuable tool for circuit design and circuit optimization. The following is a comparison of the modeled and measured results for the sweep circuit along with a discussion on using the model to understand and correct undesired circuit behavior.

**Streak Sweep Circuit Fundamental Design**

The basic circuit concept for the deflection voltage generator in the sweep module is a voltage step applied to an RLC (resistor, inductor, capacitor) series resonant circuit as illustrated in Fig. 73.10. The deflection circuit is bipolar, and each deflection plate is driven by an equivalent RLC circuit (see Fig. 73.8). The step is positive for one deflection circuit and negative for the other. This creates a voltage ramp that is twice the amplitude of that applied to one plate only. The C in the resonant circuit is formed by the capacitance of the deflection plate in the streak tube. The voltage across the capacitor (deflection plate) is given by the following exponentially decaying sinusoidal form and is illustrated in Fig. 73.11:[2]

$$V_c(t) = V_{\text{step}}\left\{1 - e^{-\alpha \cdot t}\left[\cos\left(A\ \alpha \cdot t\right) + \frac{\sin\left(A\ \alpha \cdot t\right)}{A}\right]\right\}, \quad (1)$$

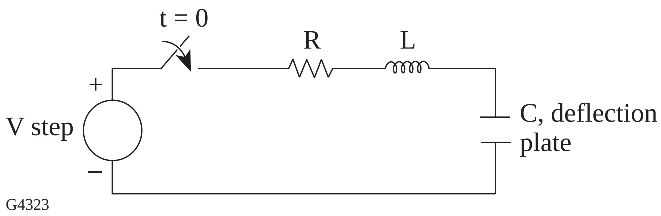


Figure 73.10
Basic RLC circuit with voltage step generator (R: resistor; L: inductor; C: capacitor).

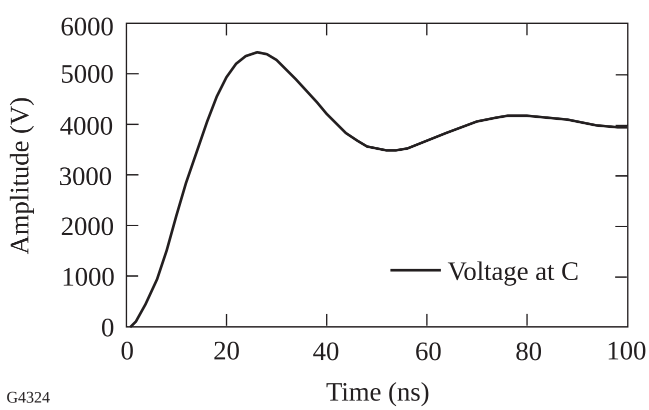


Figure 73.11
Exponentially decaying sinusoid produced by the step response of a series RLC circuit.

where

$$\alpha = \frac{R}{2L}, \quad A = \sqrt{4Q^2 - 1}, \quad Q = \frac{1}{R}\sqrt{\frac{L}{C}}.$$

$Q$ represents the quality factor of the resonant circuit. The quality factor is the power stored by the resonant circuit divided by the power dissipated per cycle of the resonant frequency.

Ideally the sweep voltage should be a linear ramp. Although the voltage waveform produced by Eq. (1) is not linear, a section of the waveform in Fig. 73.11 between $t = 0$ and the voltage peak approximates a linear ramp. The linearity of this section is within a useable degree of accuracy for the streak camera sweep. The benefit in using the RLC resonator is that the sweep ramp can be adjusted by appropriate choice of $R$, $L$, and $V_{\text{step}}$ without changing the circuit configuration. Another benefit is the low circuit complexity.

As an example of the achievable linearity, for a 4000-V step with a desired slope of 333 V/ns over a 2000-V range, the following values for $R$ and $L$ are used, given a 10-pF deflection plate capacitance: $R = 498\ \Omega$, $L = 6.3\ \mu$H. The waveform produced using these values has a slope of 306 V/ns at the start of the 2000-V sweep range (deflection plate voltage = 1340 V) and a slope of 310 V/ns at the end (deflection plate voltage = 3340 V). The center of the range has a slope of 333 V/ns as desired (deflection plate voltage = 2340 V). The slope deviates from an ideal linear slope by a maximum of 8.1% at the ends. This deviation translates into a maximum deflection-plate voltage error of 25 V, or a theoretical position error of 0.5 mm at the edges of the streak tube display used in the development. Choosing higher step voltages and higher circuit $Q$'s will reduce this error.

To create the voltage step, a fast-switching, low-jitter, high-voltage circuit that can also accommodate high peak currents is necessary. Currently, the best device for this application is an avalanche transistor. An avalanche transistor is a bipolar junction transistor that can repetitively operate nondestructively in the current-mode second breakdown region.[3] When these transistors are off, they can hold off hundreds of volts with minimal conduction between the collector and emitter. When a small amount of carriers are injected into the base, the transistor goes from minimal conduction to current-mode second breakdown operation where the equivalent impedance between the collector and emitter drops to a few ohms. This action takes place in subnanosecond time frames. The transistor used for this project is the Zetex FMMT417.[4] This transistor is specifically designed for current-mode second breakdown operation. The FMMT417 transistor has a collector-to-emitter voltage self-breakdown of 320 V. Since each transistor can hold off >300 V, seven series-connected avalanche transistors are used for each of the two 2000-V step generators needed in the streak camera sweep circuit design. In a series-configured circuit only one of the transistors in the stack needs to be triggered to cause all of the remaining transistors to go into current-mode second breakdown. A schematic diagram of one sweep circuit of the bipolar sweep network is shown in Fig. 73.12.

**Computer Modeling of the Sweep Circuit**

The computer model for the sweep circuit is developed using Intusoft IsSpice4[5]—a commercially available version of the electronics-industry–accepted circuit analysis software called SPICE (Simulation Program Integrated Circuits Especially), which is based on Berkeley SPICE 3F.2.[6] This program accepts arbitrary circuit configurations and calculates

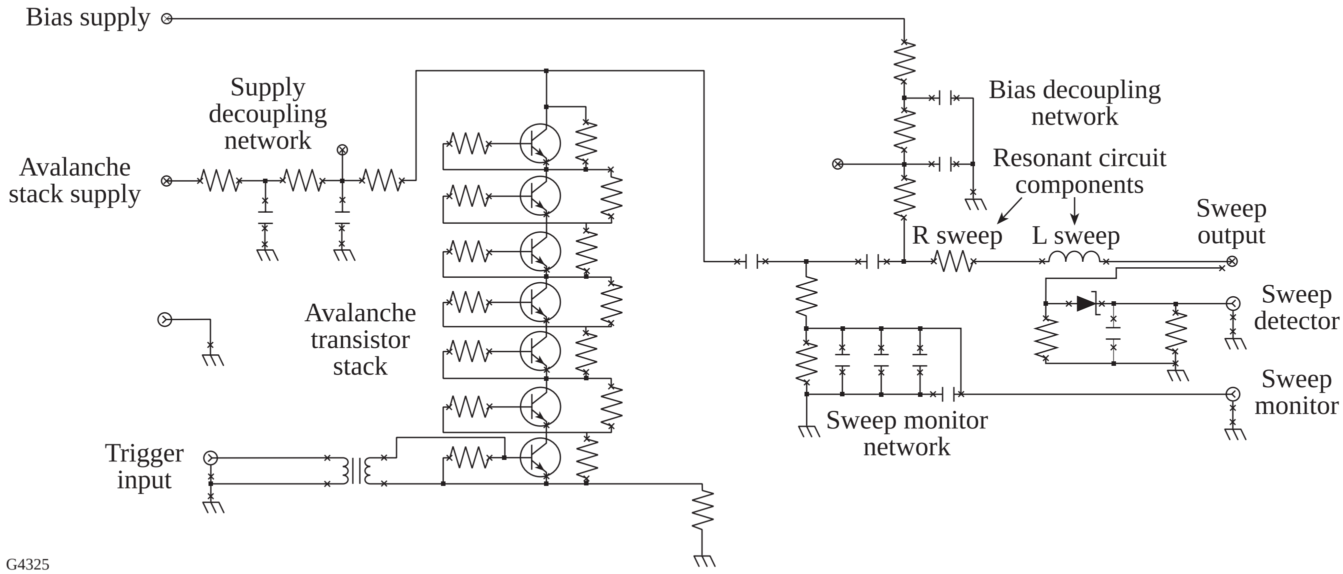


Figure 73.12
Schematic of the upper half of the multichannel streak camera sweep circuit.

currents and voltages throughout the circuit. A variety of analysis options are available in SPICE including dc, ac, and transient. For analyzing the streak sweep circuit, a transient, or time domain, analysis is performed. To simplify the model only half of the circuit is modeled, knowing that the other half provides identical results with inverted polarity. The sweep circuit is a bipolar, or balanced, configuration and can be divided into two equal parts along the line of symmetry. Each part can be analyzed independently without sacrificing accuracy. The model schematic is illustrated in Fig. 73.13.

A comparison of the schematics in Figs. 73.12 and 73.13 shows that there are significantly more components in the corresponding model network of Fig. 73.13. The components not shown in the actual circuit but shown in the model are the parasitic elements. These elements are determined through characterization of each component in the critical high-bandwidth signal path. Characterization is generally performed with calibrated test fixtures on a network analyzer. A network analyzer produces measurements of signal amplitude and phase in the frequency domain. The analyzer contains a swept calibrated signal source for excitation of the device under test and a tracking swept receiver for the measurements. One function of a network analyzer is to measure impedance of a component as a function of frequency. Care must be taken in these measurements to extract the actual component impedance from the characteristics of the test fixture. All components have parasitic lead inductance as well as capacitance to ground. Between the terminals of a component there exists parasitic capacitance. Component losses are encountered as series and parallel loss resistance. The designer must determine which of the parasitics to consider when constructing component models. Some parasitics may not affect the analysis significantly and may be omitted, but a safe rule to follow is to include any parasitics where the designer is uncertain of their effect. Once the overall circuit model is completed the parasitics can be varied to determine their effect on circuit performance.

In the model in Fig. 73.13 the avalanche stack is replaced by a pulsed voltage source, V1. This source simulates the waveform observed across the avalanche stack. The actual avalanche stack dc supply is simulated by a short circuit to ground at R12 since an ideal voltage source has 0-Ω impedance. L1 is added to simulate the combined inductance of the avalanche transistors and the interconnect wiring. R3 simulates the combined on-state resistance of the avalanche transistors in current-mode second breakdown. The network to the left of the avalanche stack simulator, including R1, R2, and R12, simulates the stack supply decoupling network with parasitics. Likewise, the network including R5, R6, and R11 forms the decoupling network with parasitics for the bias supply, V2. The *R* and *L* for the slope-forming resonant circuit are represented by R14 and L8, respectively. The right-hand connection to R10 is the output of the module. This point is followed by a high

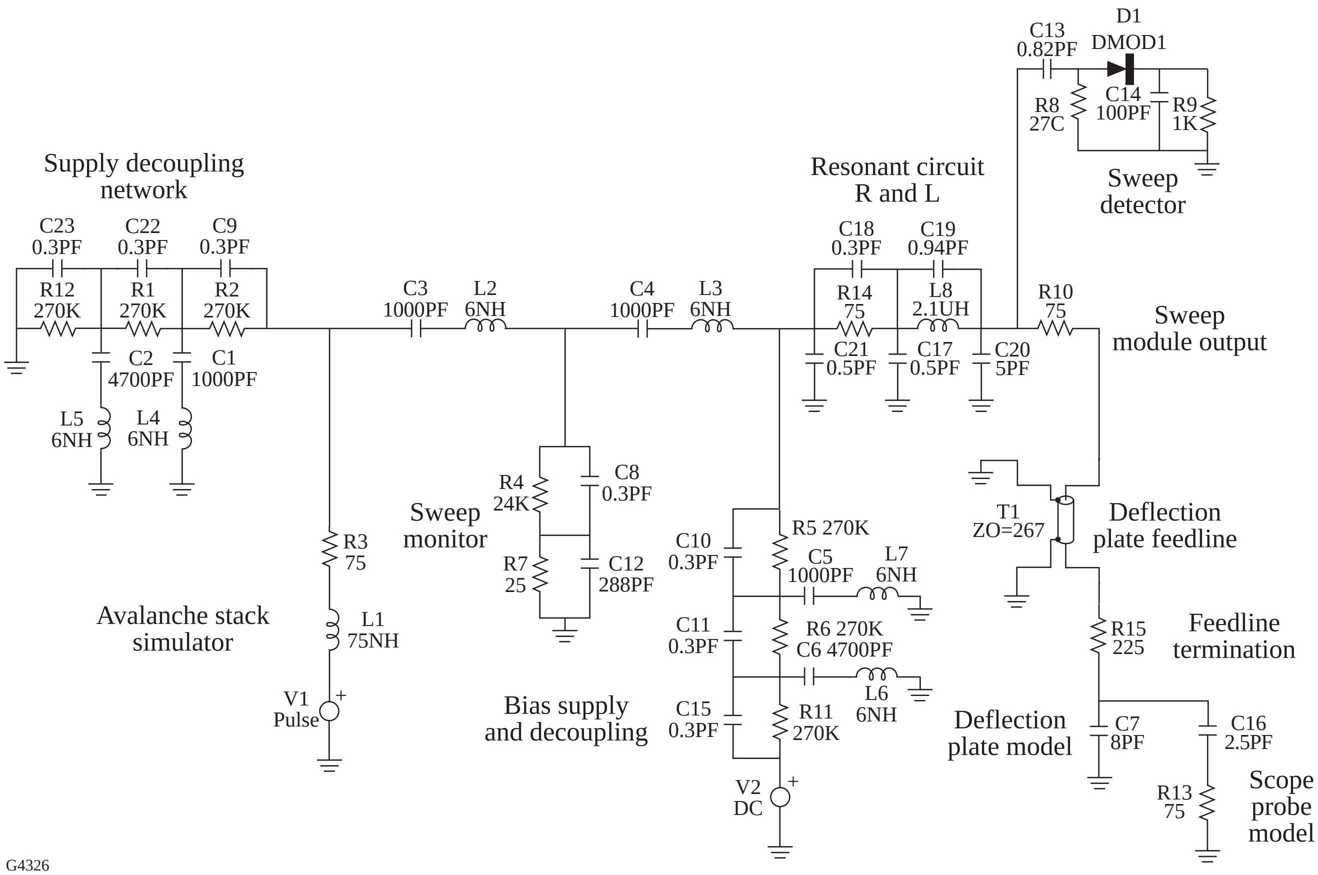


Figure 73.13
Schematic of the SPICE model for the multichannel streak camera sweep circuit.

impedance transmission line representing the feed wire to the deflection plate, C7. C16 and R13 represent a model of the oscilloscope probe used to monitor the performance of the sweep generator. The scope probe is modeled to determine its effective loading on the sweep waveform. The model also includes the sweep monitor network as well as the sweep detector network as seen in the original schematic of Fig. 73.12.

**Model Results Versus Measured Results**

Data from Figs. 73.14 and 73.15 illustrate a good correlation between the measured and model-predicted results for the sweep waveforms. The measured data is taken using a high-bandwidth oscilloscope connected to the deflection plates of the streak tube through 250-MHz-bandwidth, 100:1, high-impedance oscilloscope probes.[7,8] The plots in Fig. 73.14 are for one deflection plate voltage versus time. The other plate voltage is equivalent with opposite polarity. Figure 73.15 is the differential (slope) of the curves in Fig. 73.14. The desired theoretical slope is 167 V/ns for one deflection plate, or 333 V/ns for the differentially driven pair of plates to obtain a 6-ns sweep rate.

The curves presented are referenced in the time axis to the zero crossing of the deflection plate voltage. The illustrated curves extend past the active sweep time of 6 ns (active sweep time = −3 ns to +3 ns). Within the 6-ns time window the maximum voltage difference between the measured and modeled results is 29 V. The average slope within the window for the measured data is 167 V/ns and 168 V/ns for the SPICE data. The standard deviation of the measured slope from 167 V/ns is 14 V/ns and 10 V/ns for the SPICE model.

**Utility of the SPICE Model**

One of the fundamental uses of the SPICE model is to evaluate the performance of the sweep network with respect to the values of *R* and *L*, the sweep-rate–determining components. The initial values for these parts are determined by theoretical calculations base on Eq. (1) for the basic RLC

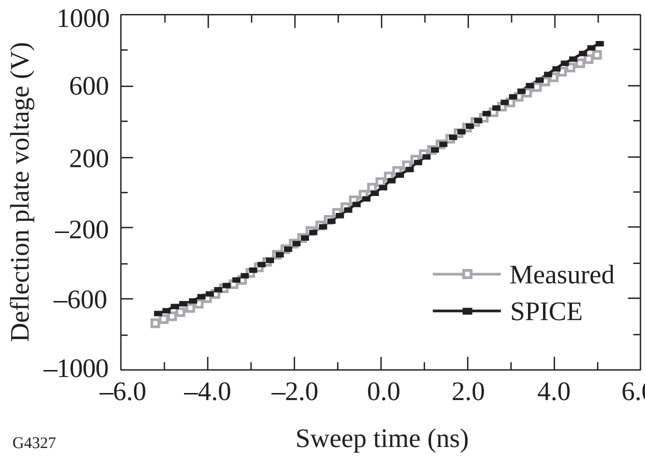


Figure 73.14
Measured sweep voltage and SPICE calculation.

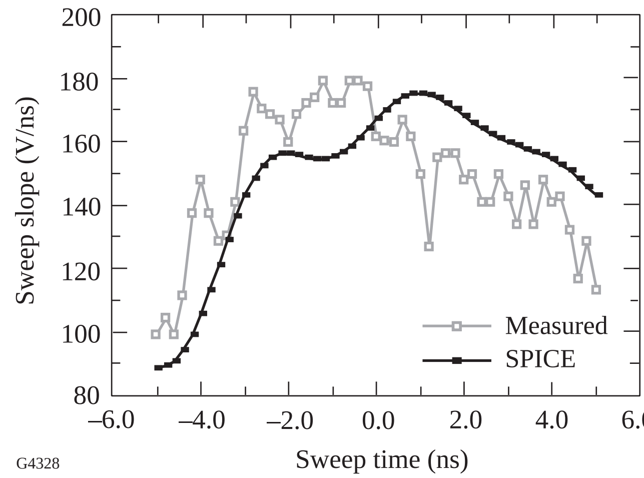


Figure 73.15
Measured sweep slope and SPICE calculation.

resonator circuit. The predicted performance of the actual circuit with the initial theoretical values can then be evaluated using the model. The values are then iteratively optimized within the model to account for the parasitics within the sweep module and streak camera. A set of values that meets the performance criteria is then determined prior to actually mounting the components in the hardware. This approach is used to develop the streak module with the results as presented in Figs. 73.14 and 73.15.

Another use for the model is to analyze and correct anomalies in the sweep waveform observed during the sweep module development. Three anomalies were found that affected the camera performance: (1) the effect of the oscilloscope probe loading on the sweep waveform; (2) a small, damped, high-frequency sinusoid superimposed on the sweep waveform; and (3) an inflection in the start of the sweep waveform.

The loading effects of the oscilloscope probes can only be evaluated experimentally by comparing the spacing of accurately timed fiducial light pulses on the streak camera output with and without the probes attached. During the streak camera development, short fiducial laser pulses with a precise period of 500 ps were applied to the photocathode of the streak tube. The pulse train from the fiducial laser appears as an intensity-modulated streak on the output screen. The distance between the peak intensity points on the output screen is directly related to the sweep rate ramp applied to the deflection plates. Comparing the distance between the peaks with and without the probes connected determines the effect of the probes on sweep rate. Using the SPICE model, a trivial effort is required to remove the simulated scope probes and calculate the change in the sweep speed. Figure 73.16 shows the change in the sweep speed as calculated by the SPICE model. The model-calculated sweep rate is 6.4 ns with the probes and 5.6 ns without. The measured sweep-rate change, using the fiducial method, is 6.6 ns with the probes and 5.6 ns with the probes removed. Good agreement is shown between the two methods. With this performance agreement the sweep-forming *R* and *L* values can be easily optimized in the model and applied to the actual circuit to compensate for oscilloscope probe loading. This is far less time consuming than optimization by iteratively changing the components in the actual sweep module and repeating the fiducial streak measurements. Also, knowing the magnitude of the probe-loading change allows actual oscilloscope-measured sweep voltage waveforms to be scaled to predict performance without the oscilloscope probe loading necessary to make the measurement.

During the initial tests of the streak camera a small sinusoidal modulation with a period of approximately 6 ns was observed superimposed on the oscilloscope display of the sweep ramp. This sinusoidal modulation was verified with streak measurements of the 500-ps-period fiducial optical timing pulse train in similar fashion to that used to determine effects of scope probe loading. Figure 73.17 shows the oscilloscope-measured sweep with the superimposed sinusoid. The model result verifies the oscilloscope measurements and is also plotted in Fig. 73.17. Figure 73.18 illustrates the verification plots from the fiducial measurements. This data agreement proves that the problem is not just an artifact of the oscilloscope measurement. From the model it has been determined that the deflection-plate feed line is acting as a constant impedance transmission line terminated by the capacitive deflection plate. This reactively terminated transmission line forms a resonant circuit that has a center frequency close to that of the superimposed sinusoid. Network analyzer measurements of the feed line indicate that it has a characteristic impedance of 267 Ω with a delay of 1.5 ns. To remove the resonance problem the feed line is made lossy through the inclusion of distributed resistance. Theoretically, this decreases the $Q$ of the resonant circuit formed by the feed line and reduces the sinusoidal current at resonance without significantly affecting the sweep ramp. Results from the model demonstrate that this approach is capable of removing the sinusoid. The plot in Fig. 73.19 is the result produced by the model with the feed line terminated to remove the resonance condition. It was later found that a lumped resistance equal to the characteristic impedance of the line could be connected in series at the deflection plate to produce the same result. This fix is supported by oscilloscope sweep waveform measurements as illustrated in Fig. 73.14.

The last problem observed relates to an inflection in the measured sweep waveforms near the start of the sweep ramp. This is again supported with the results of the model as illustrated in Fig. 73.20 near 3 ns. In this figure the time axis

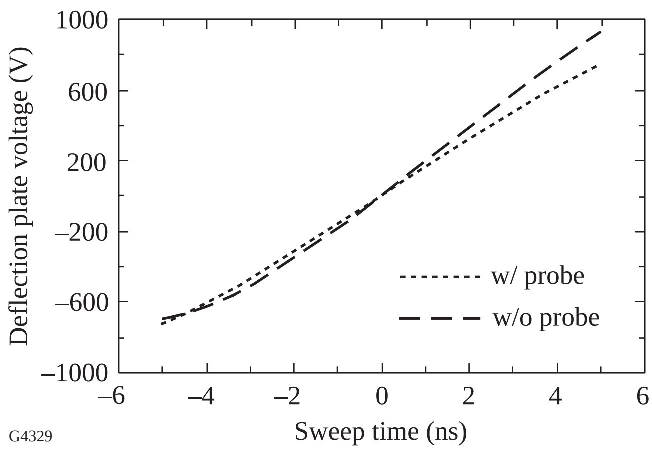


Figure 73.16
Calculated sweep-speed change with oscilloscope probe loading.

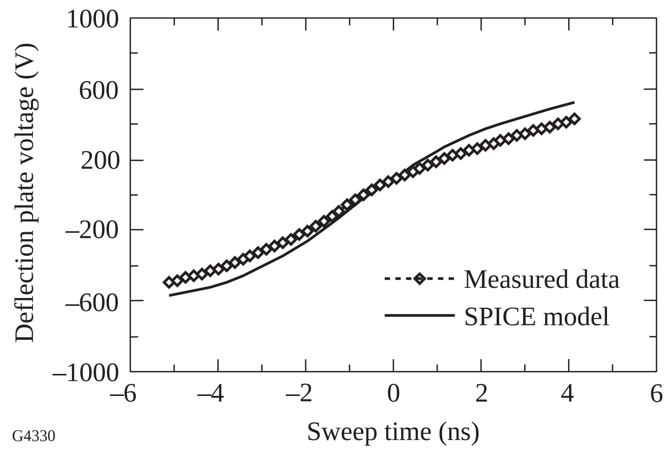


Figure 73.17
Measured sweep with superimposed sinusoid.

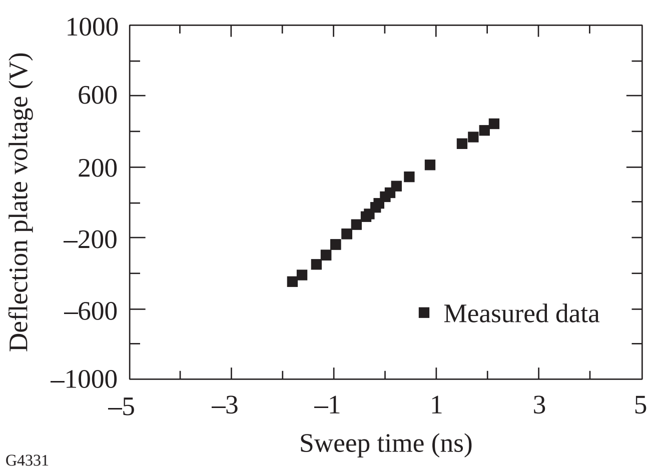


Figure 73.18
Measured sweep using optical fiducial marks.

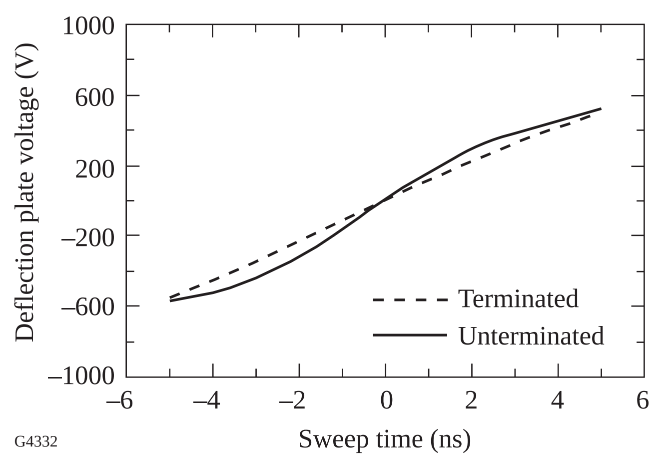


Figure 73.19
Calculated sweep with and without feed-line termination.

reference is at the start of the sweep waveform. Investigation of the inflection through its sensitivity to component value changes in the model led to the understanding of its cause. The inflection is caused by the resonance of the sweep-speed inductance (L8 in Fig. 73.13) with its parallel parasitic capacitance (C19). Using the model an investigation into the effect of the parasitic capacitance can be easily generated. It is found that a nonrealizable inductor is needed (an inductor with minimal parasitic C) to remove the inflection and that this problem cannot be eliminated. This analysis cannot be accomplished without the model since the model provides the freedom to change component characteristics outside the constraints imposed by realizable devices. Figure 73.21 shows the results of the model as the parasitic capacitance of the sweep inductor is varied. The point of this figure is that less inflection is produced by smaller parasitic capacitance.

Since the last problem is not resolvable using realizable components, the choice is made to alter the active sweep ramp range on the sweep waveform to avoid having the inflection within the active area of the sweep waveform. The operation range is altered by increasing the bias supply voltage, keeping all other circuit parameters fixed. In the waveform of Fig. 73.11, this is equivalent to setting the 2000-V active sweep ramp range to a section of the waveform closer to the peak voltage than directly in the middle between the waveform start and the peak. Care is taken to not move the range too close to the peak since linearity would be degraded at the end of the sweep ramp near the peak.

## Conclusions

In this work we show that time-domain circuit modeling and simulation of the multichannel streak camera sweep circuit using SPICE is an accurate method of analysis. The accuracy is a direct result of the attention to the parasitics for the components and interconnections in the circuitry. The parasitics, while not a severe limitation in low-frequency analysis, are a great influence to the model results in wide-bandwidth and high-frequency analysis as encountered in the sweep circuit. Component parasitic elements are generally extracted from network analyzer terminal impedance measurements on individual components and circuit interconnects. The necessary complexity of the parasitic model utilized is determined by the calculated effect of the parasitic elements within the circuit application. A SPICE circuit model, when properly constructed using the parasitic component models, is a useful tool to analyze and optimize a design. The main benefit of the model is to present a theoretical evaluation of a circuit with parasitic elements where the complexity of obtaining a closed-form analysis is intractable. Optimization using the model analysis can help greatly in reducing the effects of parasitics. The theoretical computer analysis allows rapid circuit optimization iterations as compared to equivalent hardware implementation and measurement of the change. The model is extremely valuable in diagnosing anomalies in circuit performance. An accurate model can also provide useful performance-limit analysis through ideal, parasitic-free, component substitution.

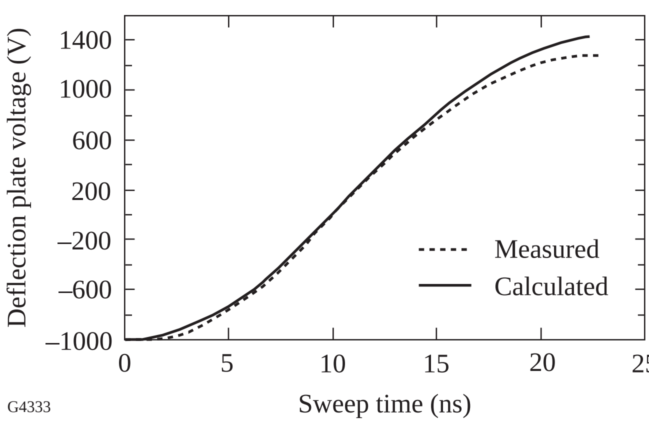


Figure 73.20
Sweep inflection.

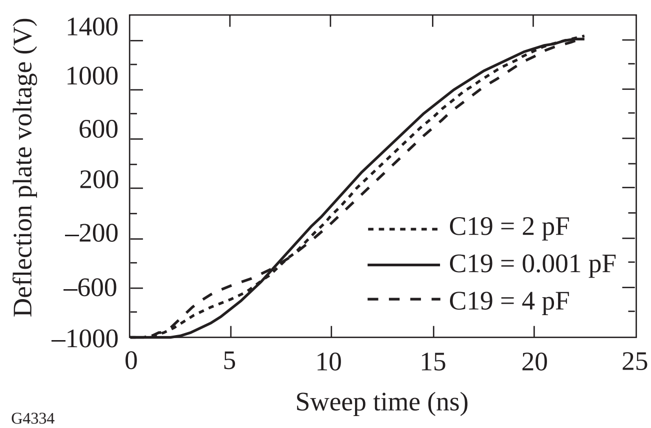


Figure 73.21
Calculated sweep with varying values of parasitic capacitance, C19, for the sweep-forming inductor, L8.

Utilizing the SPICE circuit model for the multichannel streak camera sweep module, an optimized design is developed that accommodates the component parasitics and parasitics introduced by the modular-design concept. Performance of the circuitry is optimized to remove, or accommodate, deflection-plate feedline effects, individual component parasitics, and oscilloscope probe loading. Sweep performance is optimized without the normal time-consuming change and test iterations necessary with a hardware-only approach.

## ACKNOWLEDGMENT

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